IN THE SPECIFICATION

Amendments to the Specification:

Please **delete** the title and **replace** it with the following:

"Semiconductor Device with ESD Protection for Improving the Turn-on Uniformity."

Please amend the following paragraphs as follows:

[0008] To achieve the above-mentioned object, the semiconductor device with ESD protection in accordance with the invention includes a guard ring and a MOS transistor array. In one aspect of the invention, the MOS transistor array is formed in a region surrounded by the guard ring and comprises a first MOS transistor and a second MOS transistor. In this aspect, the first MOS transistor is closer to the guard ring than the second MOS transistor is, and the channel length of the second MOS transistor is ~~greater~~ larger than that of the first MOS transistor.

[0011] In addition, a semiconductor device with an ESD protective combination according to the invention includes a first guard ring, a second guard ring, a first MOS transistor array formed in a region surrounded by the first guard ring, and a second MOS transistor array formed in a region surrounded by the second guard ring. In this aspect, the first MOS transistor array has a plurality of MOS transistors while the second MOS transistor array has a plurality of MOS transistors. The channel length of each of the MOS transistors in the second MOS transistor array is ~~greater~~ larger than that of each of the MOS transistors in the first MOS transistor array.

[0022] Referring to FIG. 3A, a semiconductor device 3 with electrostatic discharge protection in accordance with a preferred embodiment of the invention includes a guard ring 31 and a MOS transistor array 32 formed in a region surrounded by the guard ring 31. The MOS transistor array 32 includes a first MOS transistor 321, a second MOS transistor 322, a third MOS transistor 323 and a fourth MOS transistor 324. The first MOS transistor 321 is closer to the guard ring 31 than the second MOS transistor 322 is. The third MOS transistor 323 is closer to the guard ring 31 than the fourth MOS transistor 324 is. The channel length L2 of the second MOS transistor 322 is ~~greater~~ larger than the channel length L1 of the first MOS transistor 321. The channel length L4 of the fourth MOS transistor 324 is ~~greater~~ larger than the channel length L3 of the third MOS transistor 323. As shown in this drawing, the channel lengths L1, L2, L3 and L4 are the lengths of a first finger 341, a second finger 342, a third finger 343 and a fourth finger 344, respectively. The distance D1 between the first MOS transistor 321 and the guard ring 31 is equal to the distance D3 between the third MOS transistor 323 and the guard ring 31. Correspondingly, the channel length L1 is equal to the channel length L3. The distance D2 between the second MOS transistor 322 and the guard ring 31 is equal to the distance D4 between the fourth MOS transistor 324 and the guard ring 31. Correspondingly, the channel length L2 is equal to the channel length L4. In this embodiment, the above-mentioned MOS transistors are NMOS transistors, and the gates of the MOS transistors are electrically connected together. That is, the fingers are electrically connected together. In addition, the gates (or fingers) of the MOS transistors are grounded. Such a design is of a gate-grounded type.

[0027] FIG. 6 is a schematic illustration showing a circuit layout of a semiconductor device with an ESD protective combination in accordance with a preferred embodiment of the invention. Referring to FIG. 6, the semiconductor device 6 of this embodiment includes a first

guard ring 31a, a first MOS transistor array 32a formed in a region surrounded by the first guard ring 31a, a second guard ring 31b, and a second MOS transistor array 32b formed in a region surrounded by the second guard ring 31b. The first guard ring 31a is adjacent to the second guard ring 31b. The first MOS transistor array 32a has a plurality of MOS transistors and, also, the second MOS transistor array 32b has a plurality of MOS transistors. The channel length L2 of each of the MOS transistors (i.e., the length of each of fingers 341b to 344b) in the second MOS transistor array 32b is ~~greater~~ larger than the channel length L1 of each of the MOS transistors (i.e., the length of each of fingers 341a to 344a) in the first MOS transistor array 32a. Accordingly, when the direction of the electrostatic current is shown as an arrow E, the MOS transistors of the second MOS transistor array 32b and the first MOS transistor array 32a can be turned on simultaneously, thereby improving the turn-on uniformity of all MOS transistor arrays.